



Docket No.  
87552.99R134/SE-906D

**IN THE UNITED STATES PATENT & TRADEMARK OFFICE**

**AMENDMENT OF REVISED APPEAL BRIEF  
IN RESPONSE TO NOTIFICATION OF NON-COMPLIANCE**

Assistant Commissioner for Patents  
Washington, D.C. 20231  
Box AF

In response to the office communication, Notification of Non-Compliance with 37 CFR 1.192 (c), please find enclosed an Amended Appendix of claims to the Revised Appeal Brief for the above-identified application. Also enclosed is a Marked-Up Copy of the Appendix showing the changes required by the office communication.

Respectfully submitted,

Date August 23, 2001

Lee J. Fleckenstein  
Lee J. Fleckenstein  
Registration No. 36,136

JAECKLE FLEISCHMANN & MUGEL, LLP  
39 State Street  
Rochester, New York 14614-1310  
Telephone: (716) 262-0950  
Facsimile: (716) 262-4133

Paul - Bernkopf @  
~~intersil.com~~  
intersil.com

85

go 12 ind

**Amended Appendix**

Claims 1-5, 7-10, 13-22:

1. A silicon-on-insulator integrated circuit, comprising:
  - (a) a handle die;
  - (b) a substantially continuous silicide layer over said handle die,
  - (c) a substantially continuous first dielectric layer overlying one side of said silicide layer;
  - (d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;
  - (e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and
  - (f) interconnected transistors in and at the upper surface of said device silicon layer.
2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.
3. The integrated circuit of claim 1 further comprising:
  - (g) trenches extending through said device silicon layer and separating said device silicon layer into islands.
4. The integrated circuit of claim 1 wherein said device silicon layer includes deep buried layers abutting said dielectric layer.
5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and at least one of said dielectric layers comprises diamond.

7. A silicon-on insulator integrated circuit comprising:
  - (a) a handle die;
  - (b) a first dielectric layer formed on said handle die
  - (c) a substantially continuous silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;
  - (d) a substantially continuous second dielectric layer disposed between said silicide layer and a device silicon layer;
  - (e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and
  - (f) interconnected transistors in and at an upper surface of said device silicon layer.

8. The integrated circuit of claim 7 further comprising:
  - (g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.

9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about  $2 \mu\text{m}$ , and said conductive material is tungsten.

10. A bonded wafer integrated circuit comprising:
  - (a) a handle die comprising a first dielectric layer, said first dielectric layer comprising a first bonding material;
  - (b) a silicide layer bonded by said first bonding material to said first dielectric layer;
  - (c) a device wafer comprising a device layer and a second dielectric layer comprising a second bonding material, said second dielectric layer being bonded to said silicide layer and said device layer by said second bonding material; and

(d) interconnected transistors in and at a surface of said device layer;  
wherein said silicide layer comprises a third bonding material that bonds said silicide layer to said handle die and said device wafer.

13. The integrated circuit of claim 10 wherein said handle die is silicon and said first dielectric layer is silicon dioxide portion adjacent said homogeneous silicide layer].

14. The integrated circuit of claim 10 wherein said silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:

(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said first dielectric layer is a diamond layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.

19. The integrated circuit of claim 10 wherein said first and second bonding materials each comprises a thin layer of polysilicon, said polysilicon being substantially consumed during bonding.

20. The integrated circuit of claim 19 wherein said first bonding material further comprises an aqueous oxidizing solution.

21. The integrated circuit of claim 20 wherein said aqueous oxidizing solution comprises nitric acid and hydrogen peroxide.

22. The integrated circuit of claim 10 wherein said third bonding material is a silicide of a metal selected from the group consisting of cobalt, platinum, tungsten, and titanium.

**Amended Appendix**

Claims 1-5, 7-10, 13-22:

1. A silicon-on-insulator integrated circuit, comprising:
  - (a) a handle die;
  - (b) a substantially continuous silicide layer over said handle die,
  - (c) a substantially continuous first dielectric layer overlying one side of said silicide layer;
  - (d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;
  - (e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and
  - (f) interconnected transistors in and at the upper surface of said device silicon layer.
2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.
3. The integrated circuit of claim 1 further comprising:
  - (g) trenches extending through said device silicon layer and separating said device silicon layer into islands.
4. The integrated circuit of claim 1 wherein said device silicon layer includes *deep* buried layers abutting said dielectric layer.
5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and at least one of said dielectric layers comprises diamond.

7. A silicon-on insulator integrated circuit comprising:
  - (a) a handle die;
  - (b) a first dielectric layer formed on said handle die
  - (c) a substantially continuous silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;
  - (d) a substantially continuous second dielectric layer disposed between said silicide layer and a device silicon layer;
  - (e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and
  - (f) interconnected transistors in and at an upper surface of said device silicon layer.
8. The integrated circuit of claim 7 further comprising:
  - (g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.
9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about  $2 \mu\text{m}$ , and said conductive material is tungsten.
10. A bonded wafer integrated circuit comprising:
  - (a) a handle die comprising a first dielectric layer, said first dielectric layer comprising a first bonding material;
  - (b) a silicide layer bonded by said first bonding material to said first dielectric layer;
  - (c) a device wafer comprising a device layer and a second dielectric layer comprising a second bonding material, said second dielectric layer being bonded to said silicide layer and said device layer by said second bonding material; and

(d) interconnected transistors in and at a surface of said device layer; wherein said silicide layer comprises a third bonding material that bonds said silicide layer to said handle die and said device wafer.

13. The integrated circuit of claim 10 wherein said handle die is silicon and said first dielectric layer is silicon dioxide portion adjacent said homogeneous silicide layer].

14. The integrated circuit of claim 10 wherein said silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:  
(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said first dielectric layer is a diamond layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.

19. The integrated circuit of claim 10 wherein said first and second bonding materials each comprises a thin layer of polysilicon, said polysilicon being substantially consumed during bonding.

20. The integrated circuit of claim 19 wherein said first bonding material further comprises an aqueous oxidizing solution.
21. The integrated circuit of claim 20 wherein said aqueous oxidizing solution comprises nitric acid and hydrogen peroxide.
22. The integrated circuit of claim 10 wherein said third bonding material is a silicide of a metal selected from the group consisting of cobalt, platinum, tungsten, and titanium.

**Amended Appendix**

Claims 1-5, 7-10, 13-22:

1. A silicon-on-insulator integrated circuit, comprising:
  - (a) a handle die;
  - (b) a substantially continuous silicide layer over said handle die,
  - (c) a substantially continuous first dielectric layer overlying one side of said silicide layer;
  - (d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;
  - (e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and
  - (f) interconnected transistors in and at the upper surface of said device silicon layer.
2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.
3. The integrated circuit of claim 1 further comprising:
  - (g) trenches extending through said device silicon layer and separating said device silicon layer into islands.
4. The integrated circuit of claim 1 wherein said device silicon layer includes deep buried layers abutting said dielectric layer.
5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and at least one of said dielectric layers comprises diamond.

7. A silicon-on insulator integrated circuit comprising:
  - (a) a handle die;
  - (b) a first dielectric layer formed on said handle die
  - (c) a substantially continuous silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;
  - (d) a substantially continuous second dielectric layer disposed between said silicide layer and a device silicon layer;
  - (e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and
  - (f) interconnected transistors in and at an upper surface of said device silicon layer.
8. The integrated circuit of claim 7 further comprising:
  - (g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.
9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about 2  $\mu\text{m}$ , and said conductive material is tungsten.
10. A bonded wafer integrated circuit comprising:
  - (a) a handle die comprising a first dielectric layer, said first dielectric layer comprising a first bonding material;
  - (b) a silicide layer bonded by said first bonding material to said first dielectric layer;
  - (c) a device wafer comprising a device layer and a second dielectric layer comprising a second bonding material, said second dielectric layer being bonded to said silicide layer and said device layer by said second bonding material; and

(d) interconnected transistors in and at a surface of said device layer; wherein said silicide layer comprises a third bonding material that bonds said silicide layer to said handle die and said device wafer.

13. The integrated circuit of claim 10 wherein said handle die is silicon and said first dielectric layer is silicon dioxide portion adjacent said homogeneous silicide layer].

14. The integrated circuit of claim 10 wherein said silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:

(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said first dielectric layer is a diamond layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.

19. The integrated circuit of claim 10 wherein said first and second bonding materials each comprises a thin layer of polysilicon, said polysilicon being substantially consumed during bonding.

20. The integrated circuit of claim 19 wherein said first bonding material further comprises an aqueous oxidizing solution.
21. The integrated circuit of claim 20 wherein said aqueous oxidizing solution comprises nitric acid and hydrogen peroxide.
22. The integrated circuit of claim 10 wherein said third bonding material is a silicide of a metal selected from the group consisting of cobalt, platinum, tungsten, and titanium.



## Appendix (Marked-Up Copy)

Claims 1-5, 7-10, 13-22:

1. A silicon-on-insulator integrated circuit, comprising:
  - (a) a handle die;
  - (b) a substantially continuous [and unbroken] silicide layer over said handle die,
  - (c) a substantially continuous [and unbroken] first dielectric layer overlying one side of said silicide layer;
  - (d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;
  - (e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and
  - (f) interconnected transistors in and at the upper surface of said device silicon layer.
2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.
3. The integrated circuit of claim 1 further comprising:
  - (g) trenches extending through said device silicon layer and separating said device silicon layer into islands.
4. The integrated circuit of claim 1 wherein said device silicon layer includes deep buried layers abutting said dielectric layer.
5. The integrated circuit of claim 1 wherein said handle wafer comprises silicon and at least one of said dielectric layers comprises diamond.

7. A silicon-on insulator integrated circuit comprising:
  - (a) a handle die;
  - (b) a first dielectric layer formed on said handle die
  - (c) a substantially continuous [and unbroken] silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;
  - (d) a substantially continuous [and unbroken] second dielectric layer disposed between said silicide layer and a device silicon layer;
  - (e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and
  - (f) interconnected transistors in and at an upper surface of said device silicon layer.

8. The integrated circuit of claim 7 further comprising:
  - (g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.
9. The integrated circuit of claim 8 wherein said islands have a thickness no greater than about  $2 \mu\text{m}$ , and said conductive material is tungsten.

10. A bonded wafer integrated circuit comprising:
  - (a) a handle die comprising a first dielectric layer, said first dielectric layer comprising a first bonding material;
  - (b) a silicide layer bonded by said first bonding material to said first dielectric layer;
  - (c) a device wafer comprising a device layer and a second dielectric layer comprising a a second bonding material, said second dielectric layer being bonded to said

silicide layer and said device layer by said second bonding material; and

(d) interconnected transistors in and at a surface of said device layer;

wherein said silicide layer comprises a third bonding material that bonds said silicide layer to said handle die and said device wafer.

13. The integrated circuit of claim 10 wherein said handle die is silicon and said first dielectric layer is silicon dioxide portion adjacent said homogeneous silicide layer].

14. The integrated circuit of claim 10 wherein said [homogeneous] silicide layer comprises a diffusion barrier to impurities.

15. The integrated circuit of claim 10 wherein said device includes a layer of diamond adjacent said [homogeneous] silicide layer and a layer of silicon adjacent said diamond layer, said transistors being formed in and at a surface of said silicon layer.

16. The integrated circuit of claim 10 further comprising:

(e) trenches extending into said device layer and separating a semiconductor layer of said device layer into islands that isolate each of said transistors.

17. The integrated circuit of claim 16 wherein said [device layer includes a diamond layer adjacent to said homogeneous silicide layer] first dielectric layer is a diamond layer, said trenches extending to but not through said diamond layer.

18. The integrated circuit of claim 16 wherein said [homogeneous] silicide layer is conductive, said trenches extend through said silicide layer to separate said silicide layer into buried layers between said islands and said handle die, and electrical contacts extend through said device layer to said buried layers.

19. The integrated circuit of claim 10 wherein said first and second bonding materials each comprises a thin layer of polysilicon, said polysilicon being substantially consumed during bonding.

20. The integrated circuit of claim 19 wherein said first bonding material further comprises an aqueous oxidizing solution.

21. The integrated circuit of claim 20 wherein said aqueous oxidizing solution comprises nitric acid and hydrogen peroxide.

22. The integrated circuit of claim 10 wherein said third bonding material is a silicide of a metal selected from the group consisting of cobalt, platinum, tungsten, and titanium.